

WHAT IS CLAIMED IS:

1. A MOS transistor with reduced drain capacitance comprising
a drain, and
5 a lateral isolation trench extending at least partially underneath
the drain.
2. A MOS transistor of claim 1, wherein the trench is filled with air.
3. A MOS of claim 1, wherein the trench is filled with an insulator.
4. A MOS of claim 3, wherein the insulator is a high step coverable
10 insulating material.
5. A MOS of claim 4, wherein the insulator is PETEOS.
6. A MOS of claim 1, wherein the trench has a $\langle 110 \rangle$ orientation.
7. A MOS of claim 6, wherein the trench is formed in a $\langle 100 \rangle$ silicon
wafer.
- 15 8. A method of forming a laterally extending trench in a semiconductor
material underneath a drain of a MOS transistor, comprising
choosing a predetermined crystal orientation,
etching a vertically extending STI region next to the drain, and
using an anisotropic etchant to etch a trench extending laterally
20 from the STI.
9. A method of claim 8, wherein choosing the crystal orientation includes
choosing a wafer with a $\langle 100 \rangle$ orientation.
10. A method of claim 8, wherein the choosing of the crystal orientation
includes choosing a lateral trench direction that is in the $\langle 110 \rangle$ direction.
- 25 11. A method of claim 10, wherein the semiconductor material is silicon.
12. A method of claim 11, wherein the etchant is a wet anisotropic silicon
etchant.
13. A method of claim 12, wherein the etchant includes KOH.
14. A method of claim 13, wherein the etchant further includes alcohol and
30 water.

15. A method of claim 12, wherein the etchant includes TMAH.

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